Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTION:**

1. **1A**
2. **1B**
3. **N/C**
4. **1Y**
5. **1G**
6. **S**
7. **GND**
8. **2G**
9. **2Y**
10. **N/C**
11. **2B**
12. **2A**
13. **VCC-**
14. **VCC+**

**.043”**

**2 1 14 13**

**MASK**

**REF**

**7**

**K**

**12**

**11**

**9**

**.045”**

**4**

**5**

**6 7 8**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” X .004”**

**Backside Potential:**

**Mask Ref: 7K**

**APPROVED BY: DK DIE SIZE .043” X .045” DATE: 9/9/21**

**MFG: TEXAS INSTRUMENTS THICKNESS .025” P/N: 55107B**

**DG 10.1.2**

#### Rev B, 7/1